A 200 GHz Tripler Using a Single Barrier Varactor

Debabani Choudhury, *Member, IEEE,* Margaret A. Frerking, *Member, IEEE* and Paul D. Batelaan

Abstract—**In this paper, we present results for a tripler to 200 GHz using a single barrier varactor (SBV). The performance of the tripler, over an output frequency range from 186 to 207 GHz, has been measured in a crossed waveguide mount. The theoretical performance of the device and the tripler mount have been calculated using large signal analysis. An overall efficiency of 2% was achieved with efficiency at the device of above 5%. A comparison of theoretical and measured results and a discussion of various losses in the mount and the varactor are presented.**

I. Introduction

HETERODYNE receivers are used for high spectral resolution shorter-millimeter and submillimeter wave astrophysics and earth remote sensing observations. Local oscillator is one of the required components in a heterodyne receiver. One approach to provide submillimeter power for local oscillators is to use the combination of a millimeter-wave source with a frequency multiplier for harmonic generation. Frequency multipliers use a nonlinear device to generate harmonics of the input frequency from a fundamental oscillator. Although the Manley–Rowe relations show that an ideal harmonic generator with 100% efficiency is possible with a varactor, real multiplier circuits are limited by loss in the device and circuit, and by the limitations of the embedding circuitry to provide the optimum impedance terminations over a specific bandwidth at the input, output and harmonic frequencies [1], [2].

The single barrier varactor diode (SBV) is used as the nonlinear device in the multiplier presented here. It exhibits a strong nonlinearity and a symmetric C-V characteristic. To achieve the full capability of the SBV, appropriate embedding impedances must be provided by the multiplier mount. The impedances at the input and output frequencies are set to maximize coupling power into, or out of, the SBV. In higher order multipliers, current flow at the intermediate harmonics (i.e. the idler frequencies) will enhance harmonic conversion. The idler circuit requires a frequency dependent reactance for tuning the circuit over a specified bandwidth. It is these multiplier requirements together with the need for independent adjustment of the harmonic terminations (for optimum performance), that complicate the multiplier circuitry. Since the SBV has a symmetric C-V characteristic about the dc bias point, it will generate only odd harmonics, greatly simplifying the multiplier mount design. For instance a tripler mount for a symmetric device will be equivalent in complexity to a doubler mount for a device without symmetry. Similarly, a quintupler mount will be equivalent to a tripler mount, both requiring one idler.

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The authors are with the Jet Propulsion Laboratory, California Institute of Technology, 4800 Oak Grove Drive, Pasadena, CA 91109–8099.

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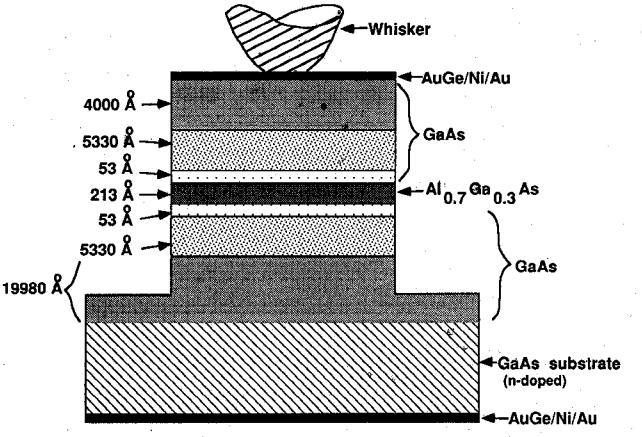

Fig. 1. Schematic of the Chalmers single barrier varactor.

II. Multiplier Device

The single barrier varactor diode, used as the multiplier device in these experiments, was developed at the Chalmers University of Technology [3], [4]. They were fabricated with the epitaxial GaAs/$Al_{0.7}Ga_{0.3}As$/GaAs material grown as indicated in Fig. 1. The $Al_{0.7}Ga_{0.3}As$ barrier is in the center having a thickness of 213 Å. On either side of the barrier, there is an undoped GaAs spacer having a thickness of 53 Å. The GaAs depletion region ($n = 1 \times 10^{17}\,\mathrm{cm}^{-3}$) on either side has a thickness of 5330 Å. Top and bottom contacts are formed on highly doped GaAs regions ($n = 3.4 \times 10^{18}\,\mathrm{cm}^{-3}$) using 1000 Å AuGe, 200 Å Ni and 1600 Å Au. The top contact is made with a whisker and the bottom is a large area ohmic contact. The conduction current through the SBV is blocked by the $Al_{0.7}Ga_{0.3}As$ barrier. Thermionic emission is the primary cause of the conduction current at moderate voltages. Variation in bias voltage changes the width of the depleted part of the moderately doped epitaxial layer, thereby forming a voltage dependent capacitance. The minimum capacitance, determined by the concentration of doping and the width of the moderately doped drift region, is obtained for maximum bias voltage. The maximum capacitance, determined by the thickness of the $Al_{0.7}Ga_{0.3}As$ barrier, is obtained at zero bias voltage. For an appropriately designed device, a capacitance swing similar to that of the Schottky-varactor diode in the reverse bias region is expected [5].

In the SBV, the maximum rf current, $i_{max} = CdV/dt$, occurs at zero bias. For zero bias, the drift regions on both sides of the barrier are undepleted. Thus the SBV devices exhibit larger losses due to dynamic series resistance than Schottky varactors. In addition, for small area devices, the ohmic contacts exhibit higher resistance than Schottky contacts. Since the second harmonic current is necessary when using Schottky

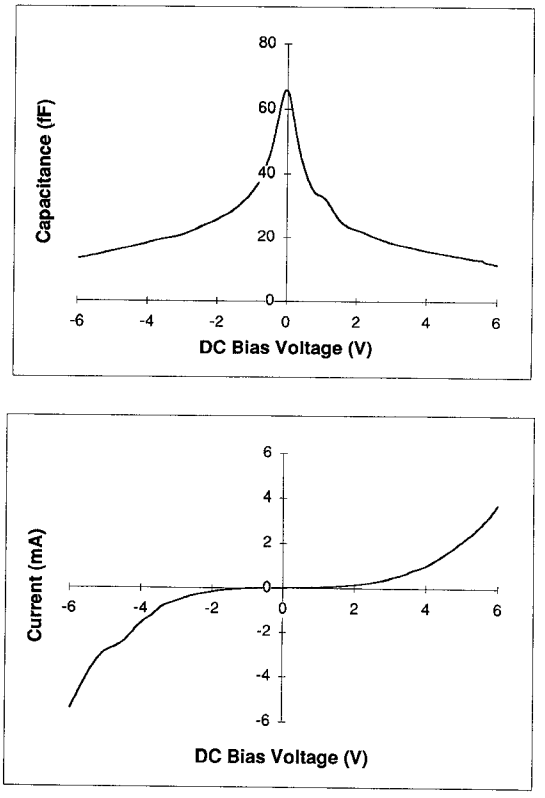

Fig. 2. Measured C-V and I-V characteristics of Chalmers single barrier varactor. The I-V characteristic is antisymmetric and the C-V characteristic symmetric, generating only odd harmonics.

diodes, conductive losses or non-optimum tuning of the idler circuit (both in the diode and in the mount circuitry) will compromise the Schottky varactor tripler performance [2], [4].

The SBV devices tested here have a mesa height of about 2.5 μm and area of $5 \times 5\,\mu\text{m}^2$. In order to evaluate the low frequency characteristic, the device has been mounted in a coaxial mount. The S-parameters were measured using a HP 8510B Network Analyzer from 1 to 20 GHz (for details of these measurements see reference [6]). The measured C-V and I-V characteristics for the $5 \times 5\,\mu\text{m}^2$ SBV diode are shown in Fig. 2. The SBV diode has a low frequency series resistance of 7 Ω. Its maximum capacitance is 65.6 fF and minimum capacitance is 12.4 fF. Based on these low frequency measurements, the cut-off frequency, given by,

$$f_c = \frac{1}{2\pi R_s}\left\{\frac{1}{C_{\min}} - \frac{1}{C_{\max}}\right\},$$

is 1200 GHz. The diodes are found to be damaged (that is the diode becomes a short circuit) when the bias voltage exceeds about 6 V.

III. Large Signal Analysis

The critical step in the multiplier analysis is to solve the voltage and current waveforms of the nonlinear device when it is pumped and biased in an arbitrary embedding network. A common solution of this nonlinear problem is to use a type of harmonic balance technique. Time-domain current and voltage solutions are sought which satisfy the diode conditions,

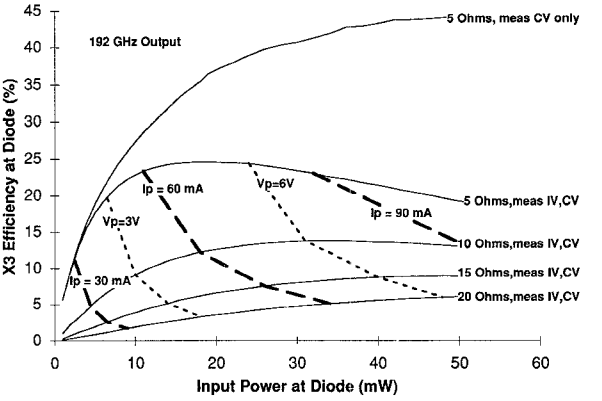

Fig. 3. Calculated tripling efficiency to 192 GHz for Chalmers single barrier varactor. Shown is the efficiency as function of input power at the diode parameterized by the series resistance varying from 5 to 20 Ω. In addition, contours of peak calculated current and voltage are indicated by the thicker and thinner dashed lines respectively.

and frequency-domain solutions are sought which satisfy the external circuit equations. In this work, a modified nonlinear program based on Siegel, Kerr and Hwang [7] has been used in order to calculate the tripling efficiency of the SBV devices. Harmonic triplers with 186 GHz, 192 GHz, 200 GHz, and 207 GHz output frequencies were calculated. The impedance at the third harmonic frequency has been optimized. The idler and the higher harmonics are set to open circuits. Impedances up to the 12th harmonic were analyzed. In the analyses, the measured C-V and I-V characteristic, shown in Fig. 2, have been used. As the C-V characteristic of a SBV device is symmetrical, no bias is needed for the large signal anlaysis. Since the series resistance is important in evaluating the device performance, the calculations were carried out for a range of resistances, 5 Ω, 10 Ω, 15 Ω and 20 Ω.

Fig. 3 presents efficiency versus input power for a SBV tripler to 192 GHz with series resistance of the device as a parameter. In order to quantify the effect of conduction current flow in the device on the multiplier performance, the performance for a device with 5 Ω series resistance was calculated assuming only a voltage variable capacitance. The theoretical efficiency is found to degrade from 45% for the purely capacitance model case to 20% when the measured I-V characteristic is included. Higher device series resistance degrades the tripler performance significantly. A series resistance of 20 Ω results in about a factor of four poorer performance than a series resistance of 5 Ω.

The breakdown voltage and saturation current limit the power handling capability of the varactors. Ideally, the peak voltage and current generated in the device should be small compared to the breakdown voltage and saturation current. In Fig. 3, superimposed over the efficiency curves, are the peak voltage and current contours generated by the large signal analysis of the SBV tripler. For comparison, the saturation current for this SBV device was calculated to be approximately 90 mA (see [8]). Based on these calculations, this occurs at an input power level greater than 35 mW. The peak voltage is less than the measured breakdown voltage 6 V at 25 mW pump power.

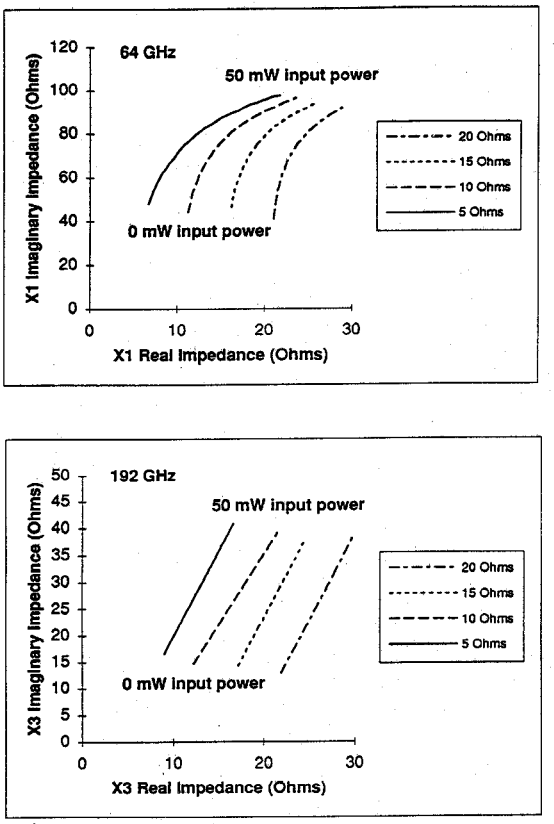

Fig. 4. Input and output circuit optimum embedding impedances calculated by the large signal analysis, parameterized by series resistance over a range of input powers.

IV. 200 GHz Waveguide Mount

An output of the large signal analysis used to optimize the device, is the embedding impedance required to maximize performance. In Fig. 4, the real part of the optimum impedance is shown on the horizontal axis and the imaginary part on the vertical axis, parameterized by the input power for both the input frequency (R_1, X_1) and the output frequency (R_3, X_3). Impedances are plotted for different series resistances of the device. Input power increases from 0 mW to 50 mW. At low input power the real part is the same as the device series resistance, while the input imaginary impedance is the impedance corresponding to the maximum capacitance at the input frequency. As the input power increases, the device capacitance decreases, increasing the imaginary impedance. The real impedances needed are in the range from 7–30 Ω. The imaginary impedances range from 40–100 Ω for the input circuit and from 15–42 Ω for the output circuit respectively.

The embedding impedances are provided to the SBV device by a crossed waveguide mount. A schematic drawing of the crossed waveguide mount is shown in Fig. 5. The SBV is mounted across the reduced height (0.99 mm ×0.254 mm) output waveguide. The output waveguide is actually oriented perpendicular to the plane of the paper. A transition to full height WR4 waveguide is integrated into the mount. A 0.71 mm wide suspended substrate low pass filter consisting of 2 μm thick Au metallization on the 76.2 μm thick quartz substrate couples the pump power from the input waveguide to

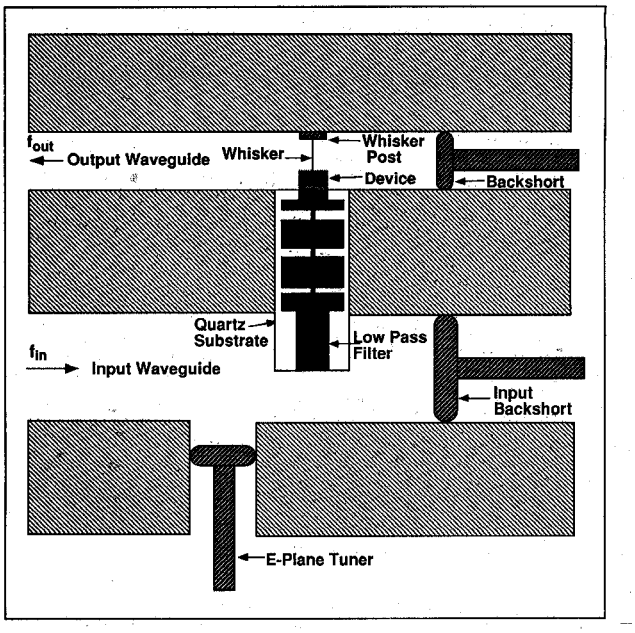

Fig. 5. Schematic diagram of the device in the crossed waveguide mount. The input waveguide is 3.81 mm × 1.91 mm half height waveguide. The output waveguide is 0.99 mm × 0.254 mm reduced height waveguide. The output waveguide is actually oriented perpendicular to the plane of the paper.

the whisker contacted SBV located in the output waveguide. An E-plane tuner and a backshort at the input waveguide provide adjustments to optimize the input embedding impedance. The output waveguide is cutoff at the input frequency. The embedding impedance at the output frequency is adjusted by varying the whisker length and by a movable backshort.

V. Experimental Results

The tripler performance was measured by using a 60–70 GHz klystron as the pump source. Since its C-V characteristic is symmetric, the device is biased at 0 V and draws no dc current. The input power is monitored by an Anritsu power meter, calibrated to measure the power at the input flange. The reflected input power is measured using a directional coupler connected to a second power meter. The third harmonic output power is measured by a third power meter. To determine the loss in the WR4 waveguide used to connect the multiplier output flange to the power meter, power was measured for two lengths of coupling WR4 waveguide. The observed loss in the WR4 output waveguide is 0.03 dB/λ, consistent with the resistive losses corresponding to the metal conductivity of $2 \times 10^7\,\Omega^{-1}\,\mathrm{m}^{-1}$. The flange-to-flange efficiency is defined as the ratio of the power at the output flange to the power available at the input flange. The efficiency and output power were measured between 186–207 GHz with three different whisker lengths, 0.152 mm, 0.213 mm and 0.279 mm. It was seen that the 25 $\mu\mathrm{m}^2$ SBV device, contacted with a 0.213 mm long whisker, gave the best tripler performance. The measured flange-to-flange efficiency versus input power at 186 GHz, 192 GHz, 196.5 GHz and 201 GHz output frequencies are shown in Fig. 6 for a 0.213 mm long whisker contact. The best performance has been achieved at 192 GHz, slightly lower than the design frequency. The flange-to-flange efficiency is more than

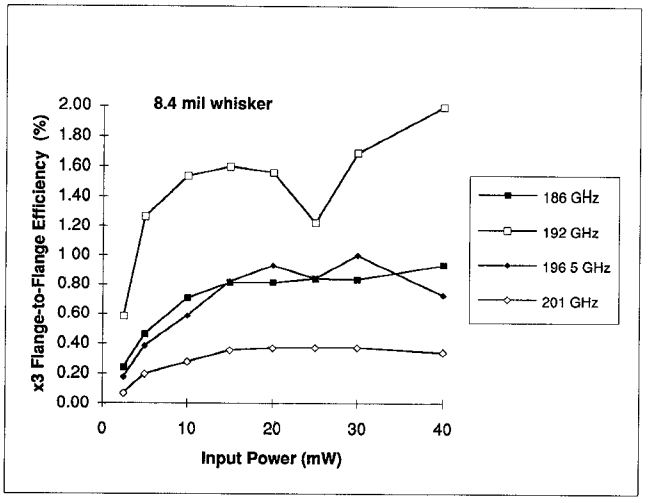

Fig. 6. Measured flange-to-flange efficiency versus input power plot for the tripler, parameterized by the output frequency.

TABLE I
LOSSES IN THE MULTIPLIER MOUNT AT OUTPUT FREQUENCY

Frequency GHz	Mismatch loss (%)	Filter loss (%)	Wave-guide loss (%)	5% BS loss (%)	10% BS loss (%)	20% BS loss (%)	Complete loss (for 10% BS loss) (%)
186	69	19	9	7	13	27	79
192	67	19	10	10	16	25	74
196	1	19	13	16	26	43	44
201	2	13	13	16	28	49	44
207	31	8	10	11	19	36	53

2% at 40 mW input power. The dip in the performance at about 25 mW input power arose from standing waves between the multiplier output and power meter. This is similar to the results demonstrated by Rydberg *et al.* using the same device [3].

To compare the experimental results to the performance predicted by the large signal analysis, the loss in the multiplier mount was assessed. Loss arises from several mechanisms. At the input frequency, the loss due to finite conductivity of the waveguide and filter and dielectric loss in the filter was calculated to be 0.6 dB using the Hewlett Packard's Microwave Design System (MDS) [9], assuming a finite conductivity of $2 \times 10^7\ \Omega^{-1}\,\mathrm{m}^{-1}$ for gold and a loss tangent of 0.0001 for quartz. The loss due to the impedance mismatch at the input, over the frequency range tested was measured to be less than 0.2 dB.

At the output frequency, the impact of the finite conductivity is higher. In addition, losses due to imperfections in the backshort are critical. Other mechanisms include the impedance mismatch and higher harmonic generation. These loss mechanisms at the output frequency have been modeled using the MDS package. The tripler mount in the MDS model includes output waveguide, a model for the whisker, the output backshort and the low pass filter. A scale model of the filter was tested giving similar results. These losses are summarized in Table I for the optimum tuning of the output backshort. The output impedance match to the diode, achieved by a combination of filter design, whisker length and backshort tuning, was optimized for the frequency range from 196 to 205 GHz, where the mismatch loss is negligible. Outside that frequency range, it is higher. The loss due to the finite conductivity in the filter is about 0.9 dB and in the waveguide wall is about 0.6 dB. In addition we have modeled several cases for a lossy output backshort, where 5%, 10% and 25% of the power is absorbed by the backshort. These losses were modeled in MDS by setting the backshort resistance, which is 0 Ω for an ideal backshort, to 4 Ω, 8 Ω and 20 Ω. The experimental results are consistent with the model assuming between 5% to 10% absorption in the backshort.

TABLE II
THE LOSS BUDGET FOR THE CROSSED WAVEGUIDE MULTIPLIER MOUNT

Output Circuit	
Finite Conductivity in Waveguide	0.6 dB
Finite Conductivity in filter	0.9 dB
Backshort Loss	1.3 dB
Impedance Mismatch	< 0.1 dB
Higher Harmonics	?
Total	2.9 dB
Input Circuit	
Finite Conductivity in filter	0.6 dB
Impedance Mismatch	0.2 dB
Total	0.8 dB

Based on these observations, the multiplier mount loss budget is presented in Table II. In the output circuit, the loss due to the finite conductivity in both the filter and the waveguide are 0.9 dB and 0.6 dB respectively. Loss due to impedance mismatch is less than 0.1 dB and loss due to backshort imperfections is 1.3 dB. Loss due to generation of higher harmonics is not known. Therefore, the loss in the output circuit is estimated to be more than 2.9 dB. Total input circuit loss is 0.8 dB. Using these loss values, 0.8 dB at input and 2.9 dB at output, the measured flange-to-flange efficiency is corrected to determine the efficiency at the diode, which is plotted in Fig. 7. Superimposed on the diode efficiency are the theoretical efficiencies calculated from the measured C-V and I-V curves for series resistances, 10 Ω, 15 Ω and 20 Ω. At low input power the measured efficiency follows the theoretical efficiency for a series resistance of about 12 Ω. The measured low frequency series resistance is 7 Ω. At 192 GHz the series resistance is expected to be somewhat higher due to the skin effect. At higher power the efficiency levels off reaching a maximum of more than 5%. This saturation corresponds to the power at which the device starts drawing conduction current. This suggests that the impact of the conductive current flow in the device on the multiplier performance is not well understood.

VI. CONCLUSION

The single barrier varactor diode has been shown to be able to provide more than 5% efficiency as a 200 GHz tripler. About 2% flange-to-flange tripling efficiency is obtained using

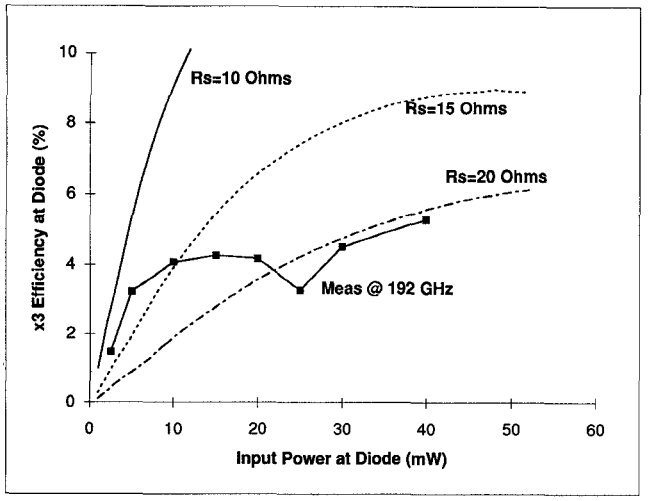

Fig. 7. Tripling efficiency at the diode versus input power plot. Shown is one measured result superimposed on three plots of theoretical predictions. At low input power, the measured data correspond to calculations for 12 Ω series resistance. As the power increases the efficiency saturates more rapidly than predicted by theory.

the crossed-waveguide tripler mount for symmetric devices. The multiplier mount has a 0.8 dB input circuit loss due to the impedance mismatch and finite conductivity in the filter. A total loss of more than 2.9 dB is estimated at the output circuit. This includes 0.6 dB and 0.9 dB losses due to the finite conductivity of the waveguide and filter, less than 0.1 dB loss due to impedance mismatch and 1.3 dB loss due to the output backshort.

We suggest that development of devices with lower leakage current will significantly improve the tripler performance. Results can be further improved by reducing the circuit losses.

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Debabani Choudhury, (M'91) received the Ph.D. degree in electrical engineering from the Indian Institute of Technology, Bombay, India, in 1991.

In July 1991, she joined the Advanced Devices Group of the Jet Propulsion Laboratory as a Post Doctoral Research Associate. At JPL, she is involved in all aspects of the submillimeter-wave solid state local oscillator development effort. Her current interests include development of solid state sources, modeling and computer-aided design of microwave, mm-wave, and submm-wave circuits, design and development of novel semiconductor devices.

Margaret A. Frerking (M'91) is a radio astronomer and submillimeter receiver design engineer. She received the B.S. and Ph.D. degrees in physics from the Massachusetts Institute of Technology. As a graduate student at MIT she built the first infrared all solid-state heterodyne receiver, using HgCdTe photo-conductors and PbSnSe lasers. She employed this receiver to observe ozone in the terrestrial atmosphere.

She initiated her astronomy career at Bell Laboratories studying protostellar star formation in dark molecular clouds. Upon joining the JPL staff in 1980, she became the cognizant engineer for the development of the 205 GHz radiometer for the Microwave Limb Sounder on the Upper Atmospheric Research Satellite. She is the principal investigator for the Submillimeter Sensors Program sponsored by NASA OAST that includes research into new solid state sources for the submillimeter regime, submillimeter SIS tunel junction mixers, and quasi-optical planar array architectures and coupling techniques. She is also a member of the JPL team responsible for the KAO water vapor radiometers which currently operates at 183, 380, and 546 GHz. In 1986 she was appointed supervisor of the Advanced Devices Group that carries out submillimeter-wave technology research.

Dr. Frerking is on the editorial board for the *IEEE Microwave and Guided Wave Letters* and the *International Journal of Infrared and Millimeter Waves.*

Paul D. Batelaan, received the B.S. degree in electronic engineering and mathematics (with honors) from California State Polytechnic College, Pomona, in 1964 and the M.S. degree in electrical engineering from the California Institute of Technology in 1965.

He joined JPL in 1965 and did radiometer development in the microwave region through 1977 and holds a NASA certificate of recognition for development of the Noise Adding Radiometer. Since 1977, he has been a member of the Technical Staff of the Microwave Observational Systems Section doing radiometer development in the millimeter and submillimeter frequency region.

Mr. Batelaan is a member of Tau Beta Pi.